

What is Claimed is:

1. A jitter-less phase detector in a clock recovery circuit comprising:
 - a first control signal generating circuit for generating a first control signal by inverting and delaying input data signals through half clock (0.5T), so that the first control signal has a pulse width starting from a transition of the data signal and lasting for half clock;
 - a second control signal generating circuit for generating a high level second control signal when the data signal changes, so that the second control signal has a pulse width starting from a transition of the data signal and terminating at a falling edge of the clock; and
 - a phase comparator for generating an up signal having a high-level from the falling edge of the first control signal to the falling edge of the second control signal when the falling edge of the first control signal is leading the falling edge of the second control signal, and generating a down signal having a high-level from the falling edge of the second control signal to the falling edge of the first control signal when the falling edge of the second control signal is leading the falling edge of the first control signal, so as to control a pair of current sources to selectively discharge and charge a capacitor.
2. The jitter-less phase detector in a clock recovery circuit as claimed in claim 1, wherein the first control signal generating circuit is formed by an inverting delay circuit of 0.5T delay and an XNOR gate; the data signal is applied to an input end of the inverting delay circuit to generate an inverting delay data signal; and the data signal and the inverting delay data signal are applied to the input ends of the XNOR gate for generating a first control signal.

3. The jitter-less phase detector in a clock recovery circuit as claimed in claim 1, wherein the second control signal generating circuit is formed by a D-type flip-flop and a first XOR gate; a clock end point of the D-type flip-flop is connected to an inverted clock signal; the data signal is applied to a data input end of the D-type flip-flop; and the data signal and an output of the D-type flip-flop are connected to input ends of the XOR gate for generating the second control signal.

4. The jitter-less phase detector in a clock recovery circuit as claimed in claim 1, wherein the phase comparator is formed by a first D-type flip-flop, a second D-type flip-flop, and an AND gate; the first control signal and the second control signal are applied to inverted clock input ends of the second and first D-type flip-flops, respectively; the data input ends of the second D-type flip-flop and first D-type flip-flop are connected to high level; outputs of the first and second D-type flip-flops generate the up and down signals; the up and down signals are sent to the input ends of the AND gate; and an output of the AND gate is connected to reset ends of the first and second D-type flip-flops, respectively.

5. The jitter-less phase detector in a clock recovery circuit as claimed in claim 1, wherein the inverted delay circuit is formed by an odd number of CMOS gates providing a path delay equal to half period of a clock.